CLAIMS

What is claimed is:

1. A signal processor for performing dyadic digital signal processing instructions having main operations and sub operations, the signal processor comprising:

at least one signal processing unit including,

a first multiplier and a first adder to execute a main operation of a dyadic digital signal processing instruction,

a second multiplier and a second adder to execute a sub operation of the dyadic digital signal processing instruction,

each of the first and second adders and the first and second multipliers having a multiplexer at its input to configure the signal processing unit to execute the main operation and the sub operation of the dyadic digital signal processing instruction, and

an accumulator having registers to couple to the first multiplier or the first adder to provide operands or store intermediate results therefrom and to couple to the second multiplier or the second adder

to provide an operand for the sub operation of the dyadic digital signal processing instruction and to store results of the sub operation, the accumulator register having a register to couple to the buffer memory to store the digital signal processed output generated by the dyadic digital signal processing instruction.

2. The signal processor of claim 1 for performing dyadic digital signal processing instructions, the signal processor further comprising:

a reduced instruction set computer (RISC) control unit and a pipeline controller to predecode the dyadic digital signal processing instruction into a plurality of preliminary instruction execution signals, and

wherein the at least one signal processing unit further includes

a plurality of final decoders coupled to a plurality of multiplexers, each of the first and second adders and first and second multipliers having an input multiplexer from the plurality of multiplexers to receive operands responsive to the selection by those of the plurality of final decoders

coupled thereto.

3. The signal processor of claim 1 for performing dyadic digital signal processing instructions, wherein,

the main operation of the dyadic digital signal processing instruction is one of the set of multiplication, addition, comparison with a minimum or maximum value, and no operation.

4. The signal processor of claim 3 for performing dyadic digital signal processing instructions, wherein,

the sub operation of the dyadic digital signal processing instruction is one of the set of multiplication, addition, comparison with a minimum or maximum value, and no operation which differs from the main operation.

5. The signal processor of claim 1 for performing dyadic digital signal processing instructions, wherein,

the main operation of the dyadic digital signal processing instruction is selected to be one of the set of multiplication, addition, comparison with a minimum or maximum value, and no operation and the sub operation of the dyadic digital signal processing instruction is selected to be a no operation.

6. The signal processor of claim 2 for performing dyadic digital signal processing instructions, wherein,

the RISC control unit includes three adders, a memory address generator, a multiplier, and a barrel shifter to predecode the dyadic digital signal processing instruction into the plurality of preliminary instruction execution signals.

7. The signal processor of claim 1 for performing dyadic digital signal processing instructions, the signal processor further comprising:

a data memory coupled to the RISC control unit and the at least one signal processing unit for storing operands and results of the execution of the dyadic digital signal processing instruction, and

a program memory coupled to the pipeline control, the program memory to store dyadic digital signal processing instructions for execution by the at least one digital signal processing unit.

8. The signal processor of claim 1 for performing dyadic digital signal processing instructions, the signal processor further comprising:

a host interface to interface to an external host computer,

an external memory interface to read and write data to an external memory,

clock and phase-locked loop to control the timing of operations of the application specific signal processor,

a memory movement engine coupled to the buffer memory to transceive data thereto and therefrom, and

wherein the at least one signal processing unit further includes,

a data typer and aligner to order the bits of the operands for execution with the main operation, a third adder to add operands together and a compressor to compress more than two operands into a pair of operands.

9. A method of performing dyadic digital signal processing (DSP) instructions, the method comprising:

fetching a dyadic DSP instruction having a main operation and a sub operation;

predecoding the dyadic DSP instruction to generate predecoded instruction signals; and

decoding the predecoded instruction signals to generate select signals to select the inputs of multiplexers of DSP functional blocks to execute the main operation and the sub

operation.

10. The method of claim 9 of performing dyadic digital signal processing (DSP) instructions, wherein,

the main operation and the sub operation are performed in parallel during the same cycle.

11. The method of claim 9 of performing dyadic digital signal processing (DSP) instructions, wherein,

the main operation and the sub operation are performed sequentially during different cycles.

12. The method of claim 9 of performing dyadic digital signal processing (DSP) instructions, wherein,

the main operation and the sub operation are two different operations selected from the set of multiplication, addition, comparison with a minimum or maximum value, and no operation.

13. The method of claim 9 of performing dyadic digital signal processing (DSP) instructions, wherein,

the DSP functional blocks include a first and second adder and a first and second multiplier, the DSP functional blocks to perform addition, subtraction and a comparison with a minimal

value or a maximum value.

14. An instruction set architecture (ISA) for execution of operations within a digital signal processor, the instruction set architecture comprising:

a set of instructions for operation within a digital signal processor wherein each instruction includes a first operand accessed directly from memory, a second operand accessed directly from memory of a local register, and a destination register to store results, the set of instructions including,

a 20-bit DSP instruction, and

a 40-bit DSP instruction,

the set of instructions to accelerate calculations within the digital signal processor of the type where D = [(A operation one B) operation two C] where operation one and operation two are separate signal processing operations.

15. The instruction set architecture (ISA) of claim 14 for execution of operations within a digital signal processor, wherein,

the twenty bit instruction uses mode bits in

control registers (i.e. mode registers) and the forty bit instruction has a control extension to override mode registers.

16. The instruction set architecture (ISA) of claim 14 for execution of operations within a digital signal processor, wherein,

the set of instructions further includes a dyadic instruction to execute two operations in one instruction .

17. The instruction set architecture (ISA) of claim 16 for execution of operations within a digital signal processor, wherein

the two operations of the dyadic instruction for execution in one instruction are DSP operations.

18. The instruction set architecture (ISA) of claim 17 for execution of operations within a digital signal processor, wherein

the DSP operations are of the set of operations of multiplication, addition, extremum, and no operation.

19. A dyadic digital signal processing (DSP) instruction

for execution in digital signal processor, the dyadic DSP instruction comprising:

a main DSP operation and a sub DSP operation to be executed in one processor cycle;

a first field indicating execution of the main DSP operation and the sub DSP operation to be executed in sequence serially or executed substantially simultaneously in parallel; and

a second field indicating a first operand, a third field indicating a second operand, and a fourth field indicating a destination.

20. The dyadic digital signal processing (DSP) instruction of claim 19 for execution in a digital signal processor, wherein

the DSP operations are of the set of operations of multiplication, addition, extremum, and no operation.